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RECENT TREND BASED WALLACE TREE MULTIPLIER AIMING TO LOW LEAKAGE POWER

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ABSTRACT

A new domino circuit is proposed with low leakage and high noise immunity which decreases the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement fast and robust circuits. The technique utilized is based on comparison of mirrored current of the pull-up network with its worst case leakage current. Thus, the power consumption and delay are reduced. A 4*4 Wallace tree multiplier is designed based on CCD (Current Comparison Domino) which uses low leakage high speed full adders. These full adders uses current comparison based domino logic to achieve low leakage and high speed. The proposed 4*4 Wallace tree multiplier using current comparison based domino logic full adders was simulated using 180nm CMOS technology which shows a relative power reduction when compared to the 4*4 Wallace tree multiplier using standard full adders.

KEYWORDS*:* Domino logic, Leakage-tolerant, Noise immunity, Wallace Multiplier, Wide fan-in.

INTRODUCTION

Dynamic logic is distinguished from so-called static logic in that dynamic logic uses a clock signal in its implementation of combinational logic circuits. The usual use of a clock signal is to synchronize transitions in sequential logic circuits. For most implementations of combinational logic, a clock signal is not even needed. In contrast, in dynamic logic, there is not always a mechanism driving the output high or low. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used or refreshed before the charge in the output capacitance leaks out enough to cause the digital state of the output to change, during the part of the clock cycle that the output is not being actively driven. Dynamic logic, when properly designed, can be over twice as fast as static logic. It uses only the faster N transistors, which improve transistor sizing optimizations. Static logic is slower because it has twice the capacitive loading, higher thresholds, and uses slow P transistors for logic. Dynamic logic can be harder to work with, but it may be the only choice when increased processing speed is needed. In Dynamic logic, problem arises when cascading one gate to the next. In order to cascade dynamic logic gates, one solution is Domino Logic, which inserts an ordinary static inverter between stages. While this might seem to defeat the point of dynamic logic, since the inverter has a pFET, there are two reasons it works well. First, there is no fanout to multiple pFETs. The dynamic gate connects to exactly one inverter, so the gate is still very fast. And since the inverter connects to only nFETs in dynamic logic gates, it too is very fast. Second, the pFET in an inverter can be made smaller than in some types of logic gates.

In this paper, a new current-comparison-based domino (CCD) [1] circuit for wide fan-in applications in ultradeep submicrometer technologies is proposed. The novelty of the proposed circuit is that our work simultaneously increases performance and decreases leakage power consumption. With this, a low leakage Wallace tree multiplier [2] is designed to show its minimum power consumption.

The rest of this paper is arranged as follows. After the existing system in Section II, the proposed circuit is described in Section III. Section IV includes simulation results for the proposed circuit using 180nm CMOS tool compared with other conventional circuits. Section V concludes the results.

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EXISTING SYSTEMS

The most common domino logic is the conventional Standard Footless Domino (SFLD) as shown in Fig 1. In this design, a pMOS keeper transistor is employed to prevent any undesired discharging at the dynamic node due to the leakage currents and charge sharing of the pull-down network (PDN) during the evaluation phase, hence improving the robustness. Keeper transistor upsizing is a conventional method to improve the robustness of domino circuits. However, as the keeper transistor is upsized the contention between the keeper transistor and the evaluation network increases in the evaluation phase. This causes an increase in the evaluation delay of the circuit, increase in power consumption and degradation of performance. Therefore, to improve noise and leakage immunity, keeper upsizing is used as a compromise between delay and power. The keeper ratio *K* is defined as

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{Keeper-transistor}}{\mu_n \left(\frac{W}{L}\right)_{Evaluation-transistor}} \quad (3)$$

where W is the width of the transistor and L is the length of the transistor and μ_n and μ_p are the electron and hole mobilities respectively.

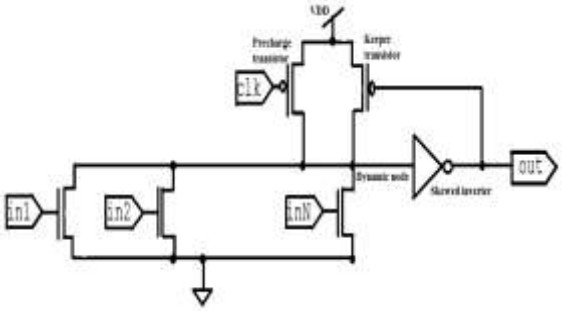

Fig. 1 Standard Footless Domino

Several circuit techniques are proposed in the literature to address these issues. In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD) [4] , high speed domino (HSD) [5] , LCR Keeper [6] as shown in Fig. 2(a), 2(b) and 2(c) respectively.

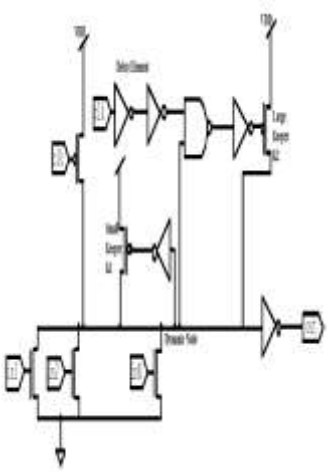

Fig. 2 a) CKD

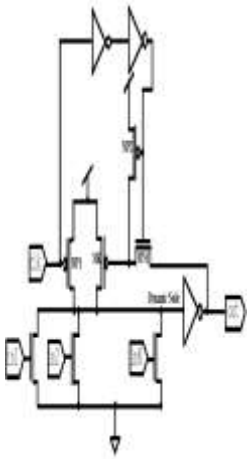

Fig. 2 b) HSD

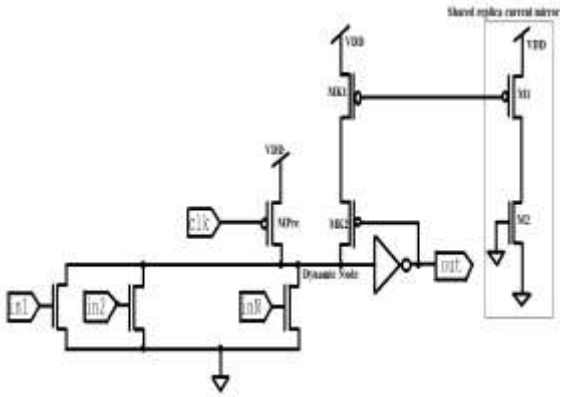

Fig.2 c) LCR Keeper

The drawbacks analysed with the existing works are increase in leakage current, noise immunity, decrease in contention current robustness, power consumption, delay etc.,

PROPOSED CCD IN WALLACE TREE MULTIPLIER

In wide fan-in gates, the speed is decreased due to the capacitance of the dynamic node is large. Upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems could be resolved if the PDN implements logical function, is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with the worst case leakage current. This concept of CCD [1] is illustrated in Fig. 2(a). where PUN is used instead of PDN.

Transistor *MK* is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage. Another important issue is the generation of reference voltage, which is the correct variation of

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the reference current according to the process variations inorder to maintain the robustness of the proposed circuit.

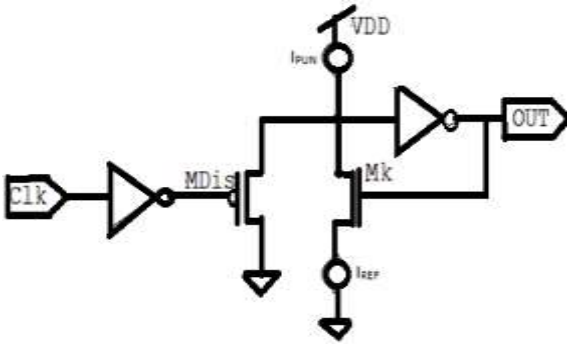

Fig. 2 a) Concept of proposed CCD design

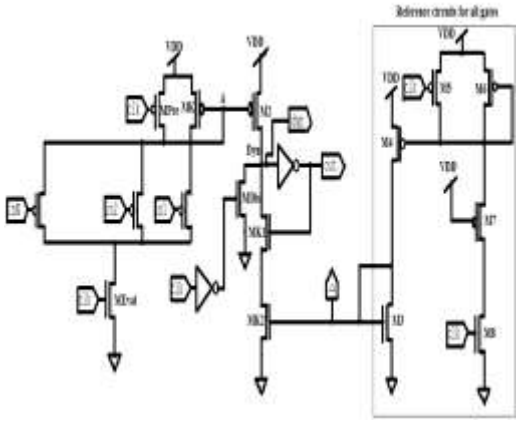

Fig. 2 b) Implementation of wide fan-in OR gate using CCD

Predischarge Phase

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", CLK = "1" in Fig. 2(b)] in this phase. Hence, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor MDis and raised to the high level by transistor Mpre, respectively. Hence, transistors Mpre, MDis, Mk1, and Mk2 are on and transistors M1, M2, and MEval are off. Then, the output voltage is raised to the high level by the output inverter.

Evaluation Phase

In this phase, clock voltage is in the high level [CLK = "1", CLK = "0" in Fig. 2(b)] and input signals can be in the low level. Hence, transistors Mpre and MDis are off, transistorM1, M2, Mk2, and MEval are on, and transistor Mk1 can be come on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. It is clear that upsizing the transistor M1 and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation.

A 4*4 Wallace tree multiplier [2] is designed using current comparison based domino logic full adders.4*4 Wallace multiplier has 12 full adders, where all these full adders are replaced by current comparison based domino logic full adders. By these adders dynamic power dissipation in the multiplier is reduced such that half of the total leakage power in the 4*4 Wallace tree multiplier is reduced. The concept of current comparison based domino logic is shown in figure 2.a. Generally process variations are due to random and systematic parameter fluctuations. Here the full adder is designed by current comparison based domino logic which uses the replica keeper current method to track the leakage current.

SIMULATION RESULTS AND COMPARISONS

The proposed circuit was simulated using 180nm CMOS technology. Figure 3 shows the graphical illustration of the comparison of power consumption between various domino OR logics. It shows a reduction in normalized power consumption from 10% to 39% compared to the SFLD. The comparison of delay of various domino logic for wide fan-in OR gates are illustrated in Figure 4. The results obtained indicate that 1.77 to 1.92 times improvement over the SFLD, indicating that the proposed circuit has a less delay compared with the rest.

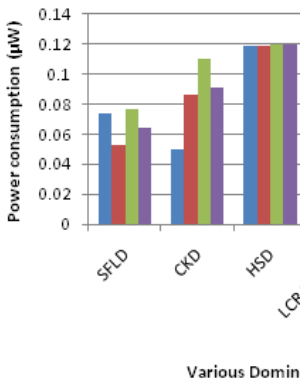

Fig 3: Comparison of Power consumption of the various domino OR logic circuits

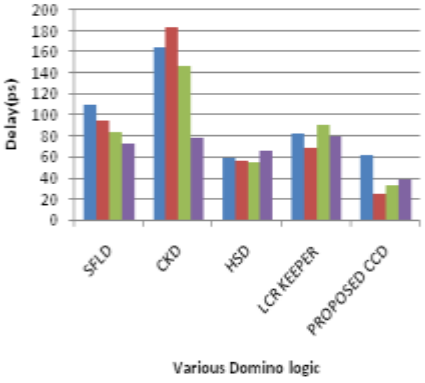

Fig 4 Comparison of Delay of the domino OR logic circuits

Figure 5 shows the schematic of CCD in full adder (CCDFA).The full adder operation equations presented below can be stated as follows: given the three 1-bit inputs A, B and Cin which calculate two 1-bit outputs Sum, for sum and Cout for carry out.

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$$Sum = A\ XOR\ B\ XOR\ C_{in} \quad (2)$$

$$C_{out} = A\ XOR\ B + B\ XOR\ C_{in} + C_{in} \quad (3)$$

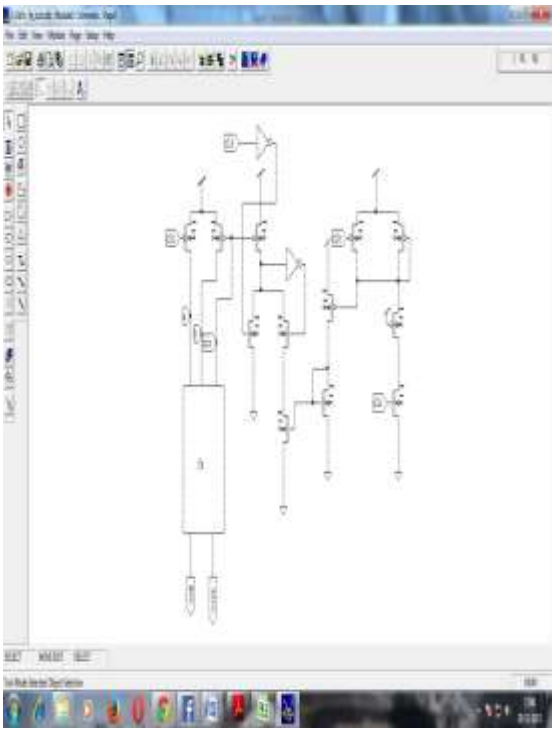
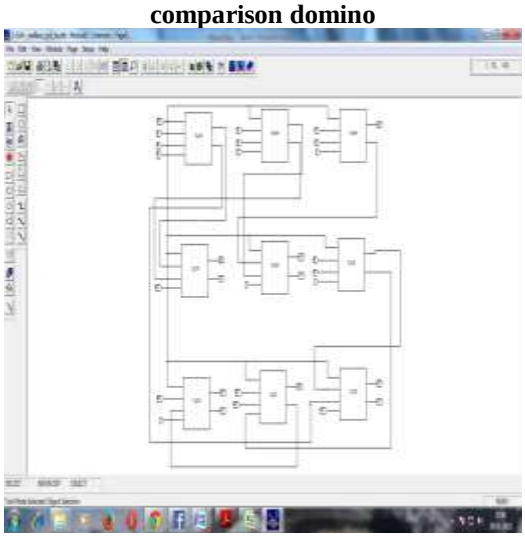


Fig 5: Schematic of full adder using current comparison domino



CONCLUSION

In this paper, a new Current Comparison based Domino (CCD) is introduced which reduces the leakage power and increases the speed of the circuit for wide fan-in logics. The main goal was to make the domino circuits more robust and with low leakage without significant performance degradation or increased power consumption. In order to reduce the leakage power, we present current comparison based domino logic 4*4 Wallace tree multiplier. From the simulation results, it can be concluded that the total leakage power has been drastically reduced by reducing half of the dynamic power dissipation.

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AUTHOR BIBLOGRAPHY

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